UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
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ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/628,769	MARISETTY ET AL.
	Examiner	Art Unit
	Gabriel L. Chu	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _21 January 2009_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _89-104_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _89-104_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _28 July 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

2.   Claim 100 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3.   Referring to claim 100, it is not clear what is intended, but Examiner will examine this claim as "the processor detects the detected error".

Claim Objections

4.   Claims 89, 94 objected to because of the following informalities:

Referring to claim 89, "an first" should be "a first".

Referring to claim 94, "routine to save a status" is understood to refer to "routine saves a status".

Referring to claim 99, "correct" should be "corrected".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

**6.   Claims 89, 93, 94 rejected under 35 U.S.C. 103(a) as being unpatentable
over US 5740357 to Gardiner et al. in view of US 5781750 to Blomgren et al.**

7.   Referring to claim 89, Gardiner discloses a processor (From line 61 of column 3,
"a service element 14, e.g. a disk drive, a CPU, etc...") comprising:

        first logic to detect an error (Figure 2, error detector 30.);

        a first interface to a first error handling routine to be invoked by the processor via
the first interface when the second logic cannot correct the detected error (From line 44
of column 6, "If the recovery is not successful, a fail response and error report (if
applicable) is sent to the next higher level." Further, from line 55 of column 8, "In
addition to the analyzer function 41 having access to lower level entities, the access
function 43 allows management of the local level error handler 40 by a higher level
entity 12. Some of this management of the local level error handler 40 includes reading
and writing of a scratch pad function 42 that serves as temporary storage of error, state,
and status information; access to and control of analyzer function 41 attributes, such as
counters and error handling thresholds; switching the reporting function 44 to report to
the tester 60 instead of to the fault handler 50, or to the next higher level entity; and for
diagnostic purposes, the higher level entity 12 may change the reporting function 44 to
report only to the tester 60 via the access function 43.").

        Although Gardiner does not specifically disclose a first memory that stores a set
of procedures to access the processor and the first error handling routine (thereby
making it software), memory to store code to access a processor is known in the art. An
example of this is shown by Blomgren, from the abstract, "Emulation mode is entered

upon reset, and performs various system checks and memory allocation. A special emulation driver is loaded into a portion of main memory set aside at reset. Software routines to emulate the more complex instructions of the CISC architecture using RISC instructions are also loaded into the emulation memory." A person having ordinary skill in the art at the time of the invention could have been motivated to have such memory and code because, from line 46 of column 3 of Blomgren, "it would be a tremendous competitive advantage to be able to run native x86 code on a RISC CPU". Further, such a component may function as a device in Gardiner's functional hierarchy, operating between the processor and whatever is attempting to natively access the processor.

8.   Referring to claim 93, see rejection of claim 89. Further note that, for example, from line 15 of column 2, Blomgren discloses that such microcode routines are stored in ROM.

9.   Referring to claim 94, Gardiner in view of Blomgren discloses the first firmware error handling routine to save a status of the detected error and at least a portion of the processor's state information (Gardiner, from line 31 of column 6, "Second, there can be a failure in a lower level with the associated error report being received from the lower level together with the fail response.").

10.   Claims 90-92, 95, 97 98 rejected under 35 U.S.C. 103(a) as being unpatentable over Gardiner and Blomgren as applied to claim 89 above, and further in view of US 5594905 to Mital.

11.   Referring to claim 90, Gardiner a second error handling routine to be invoked by the processor when the first software error handling routine cannot correct the detected

(Gardiner discloses additional functional layers, each with its own error handling routine. See for example figure 1, which shows service elements in service to each other through a functional hierarchy.).

Although Gardiner in view of Blomgren does not specifically disclose what this next layer may be or that the second error handling routine is software, such a software layer is known in the art. An example of this is shown by Mital, from line 60 of column 3, "The computer system 10 further includes firmware 18 formed at a hardware abstraction layer (HAL) intermediate of CPU 12 and hardware 16. HAL firmware 18 provides an interface between low level system software of the CPU and hardware dependent software that runs on the hardware. It is common for the firmware and hardware components of the computer system to be made by one manufacturer and the operating software to be developed by another manufacturer. The HAL firmware 18 enables essentially the same CPU operating system to run on many diverse types of underlying hardware. Here, when hardware 16 generates an interrupt, it is channeled through HAL firmware 18 which packages the hardware interrupt in a format that can be recognized by CPU 12." A person having ordinary skill in the art at the time of the invention could have been motivated to use a HAL because, as disclosed by Blomgren, "The HAL firmware 18 enables essentially the same CPU operating system to run on many diverse types of underlying hardware."

Further, Applicant uses broad "first memory" and "first interface" language, which could broadly be interpreted to encompass one or more memories or interfaces, or anywhere such software is stored and how they must be accessed. In other words, this

is merely grouping and provides no substantial structure. However, Examiner further notes that while Blomgren loads the routines into emulation memory and Mital stores in firmware (which clearly must be loaded into execution memory), Blomgren further discloses, from line 6 of column 7, "Microcode can be minimized or even eliminated because complex instructions are supported by algorithms stored in emulation memory. These algorithms are not merely microcode stored off chip, which would require much more memory, but are higher-level routines composed of RISC instructions and extended instructions." This indicates that although routines may be loaded from off-chip, it really could have been stored anywhere that is CPU accessibile, and clearly, as any code on the system, particularly such emulation and HAL code, would have to be run by the processor, it must ultimately be accessible by the processor. As such, it would have been obvious to store code anywhere that was accessible, including, for example, the memory for the HAL firmware.

12.   Referring to claim 91, Gardiner in view of Blomgren and Mital discloses a second interface to a second memory that stores an operating system (From line 18 of column 1 of Mital, "In the design of operating systems, designers often attempt to develop operating software that can run on many diverse hardware platforms."), wherein the operating system includes a third software error handling routine to be invoked by the processor when the second software error handling routine cannot correct the detected error (Gardiner discloses additional functional layers, each with its own error handling routine. See for example figure 1, which shows service elements in service to each other through a functional hierarchy. Gardiner, from line 44 of column 6, "If the recovery

is not successful, a fail response and error report (if applicable) is sent to the next

higher level.").

13.   Referring to claim 92, Gardiner in view of Blomgren and Mital discloses a first

interface to a second memory that stores an operating system (From line 18 of column

1 of Mital, "In the design of operating systems, designers often attempt to develop

operating software that can run on many diverse hardware platforms."), wherein the

operating system includes a third software error handling routine to be invoked by the

processor when the second software error handling routine cannot correct the detected

error (Gardiner discloses additional functional layers, each with its own error handling

routine. See for example figure 1, which shows service elements in service to each

other through a functional hierarchy. Gardiner, from line 44 of column 6, "If the recovery

is not successful, a fail response and error report (if applicable) is sent to the next

higher level.").

14.   Referring to claim 95, 97, see rejection of claim 90. Further note that HAL is

explicitly firmware.

15.   Referring to claim 98, see rejection of claim 92.

16.   **Claim 96 rejected under 35 U.S.C. 103(a) as being unpatentable over**

Gardiner and Blomgren and as applied to claim 94 above, and further in view of

US 5787095 to Myers et al.

17.   Referring to claim 96, Gardiner discloses saving additional state information

(From line 36 of column 6 of Gardiner, "Additional information may be gathered from the

lower level error handler 40 via the control 70.").

Although Gardiner and Blomgren do not specifically disclose the second firmware error handling routine to determine the severity of the detected error by analyzing the processor's saved state information and the detected error, determining severity by looking at state information is known in the art. An example of this is shown by Myers, from line 53 of column 19, "In a preferred embodiment, all errors or anomalous behavior is classified into one of two severity levels based on whether data integrity is compromised. The following defines the error severity levels: error notices and fatal errors." A person having ordinary skill in the art at the time of the invention could have been motivated to determine severity because, as shown in column 19 line 57 to column 20 line 31 of Myers, it allows different actions to be taken.

18.   **Claim 99, 100 rejected under 35 U.S.C. 103(a) as being unpatentable over Gardiner, Blomgren, and Mital as applied to claim 98 above, and further in view of Official Notice.**

19.   Referring to claim 99, although Gardiner, Blomgren, and Mital do not specifically disclose the processor is reset if the detected error cannot be corrected by the third error handling routine, resetting when an OS fails is very well known in the art. Examiner takes official notice for restarting an OS because of OS failure, an example of which is restarting because of a blue screen of death. A person having ordinary skill in the art at the time of the invention could have been motivated to reset after an OS fails, and in view of Gardiner that OS would have had error handling capabilities that must have failed, because the person still wants to be able to use the computer instead of never using the computer again.

20.   Referring to claim 100, Gardiner discloses the processor detects the detected

error (For example from figure 2, the error detector 30 is shown internal to the element

14.).

21.   Claims 101, 102 rejected under 35 U.S.C. 103(a) as being unpatentable over

Gardiner, Blomgren, and Mital.

22.   Referring to claim 101, see rejection of claims 89 and 90, wherein Blomgren's

emulation operates as a PAL and Mital's HAL operates as a SAL.

23.   Referring to claim 102, see rejection of claim 94.

24.   Claim 103, 104 rejected under 35 U.S.C. 103(a) as being unpatentable over

Gardiner, Blomgren, and Mital as applied to claim 102 above, and further in view

of US 5787095 to Myers et al.

25.   Referring to claim 103, Gardiner discloses saving additional state information

(From line 36 of column 6 of Gardiner, "Additional information may be gathered from the

lower level error handler 40 via the control 70.").

Although Gardiner and Blomgren do not specifically disclose the second firmware

error handling routine to determine the severity of the detected error by analyzing the

processor's saved state information and the detected error, determining severity by

looking at state information is known in the art. An example of this is shown by Myers,

from line 53 of column 19, "In a preferred embodiment, all errors or anomalous behavior

is classified into one of two severity levels based on whether data integrity is

compromised. The following defines the error severity levels: error notices and fatal

errors." A person having ordinary skill in the art at the time of the invention could have

been motivated to determine severity because, as shown in column 19 line 57 to

column 20 line 31 of Myers, it allows different actions to be taken.

26.   Referring to claim 104, see rejection of claim 92.

Conclusion

27.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-

3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00

PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

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/Gabriel L. Chu/
Primary Examiner
Art Unit 2114

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